REMARKS

Claims 1-68 are cancelled, and Claims 69-93 are added. It necessarily follows, therefore, that Claims 68-93 are pending in the application. Applicant respectfully requests examination of such pending claims.

Respectfully submitted,

Dated: Aug. 1, 2001

By: Bernard Berman
Bernard Berman
Reg. No. 37,279

09780201 . 080101

SPECIFICATION

The specification has been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

At p. 1, before the "Technical Field" section insert:

RELATED PATENT DATA

This patent is a divisional application of U.S. Patent Application Serial No. 08/996,325 which was filed on December 22, 1997, which is a continuation application of U.S. Patent Application Serial No. 08/506,084, filed July 24, 1995 which is now U.S. Patent No. 5,700,727.

CLAIMS

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

Cancel Claims 1-68.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PRIORITY Application Serial No. 08/996,325
PRIORITY Filing Date ..... December 22, 1997
Inventor ..... H. Montgomery Manning
Assignee ..... Micron Technology, Inc.
PRIORITY Group Art Unit 2822
PRIORITY Examiner ..... M. Trinh
Attorney's Docket No. MI22-1698
Title: Methods of Forming Thin Film Transistors

VERSION WITH MARKINGS TO SHOW CHANGES MADE IN THE PRELIMINARY AMENDMENT

AMENDMENTS

In the Specification

Please replace the Abstract on pages 26-27 with the following clean replacement Abstract. Applicant respectfully asserts that the following paragraph is in accordance with 37 C.F.R. § 1.72(b).

--Methods of forming thin film transistors, and transistors therefrom, are provided where at least one of the source or drain region is conductively doped while conductivity doping of the channel region is prevented without any masking by any separate masking layer. Methods include, providing a substrate having a conductive node; providing a first dielectric layer, a gate layer over the first layer and a second dielectric layer over the gate layer; providing a contact opening through the first and second layers and the gate layer, the opening defining projecting sidewalls; providing a gate dielectric layer within the opening; providing a layer of semiconductive material over the second layer, against the gate dielectric layer and in electrical communication with the node; the material defining a channel region; and conductively doping the semiconductive material layer lying outwardly of the contact opening to form one of a source region or a drain region.--

A marked up version showing amendments is provided in one or more accompanying pages separate from this amendment in accordance with 37 C.F.R. § 1.121(b)(1)(ii).

Respectfully submitted,

Dated: Sept 5, 2001

By: Bernard Berman

Bernard Berman

Reg. No. 37,279